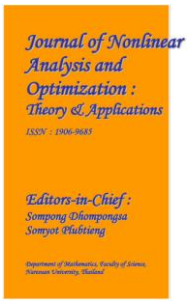
Journal of **N**onlinear **A**nalysis and **O**ptimization
Vol. 14, Issue. 2, 2023
ISSN : **1906-9685**



ESTIMATION OF POWER AND DELAY OF CMOS PHASE DETECTOR AND PHASE-FREQUENCY DETECTOR USING NANO DIMENSIONAL MOS TRANSISTOR

[1]A.Manisha ,[2]G.Nikitha,[3]E.Bhanu Prakash,[4]Dr.K.V. Ramprasad
[1,2,3]IV Year Student,[4]Assistant Professor
Department of ECE
Visvesvaraya College Of Engineering & Technology,Ibrahimpatnam,Telangana

ABSTRACT
In this paper the design of phase detector circuit using nano dimensional transistor
has been presented. which are mainly used in phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate
well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units.
The conventional circuit of phase-frequency detection has been realized and presented. The circuit schematics are simulated with the help of Tanner SPICE software. The power dissipation, transistor delay, product of power and delay of the phase detector circuit has been estimated. Power and speed performance analysis is carried out varying the value of VDD in the range 1.2 V - 5V and aspect ratio of PMOS to NMOS from 1 to 5 . Moreover, the power, gate delay and PDP of the phase-frequency detector has been designed. The results are pleasing context to the design of Very Large Scale Integrated
(VLSI) circuit having high speed and low power dissipation.

I. INTRODUCTION TO VLSI

VLSI TECHNOLOGY VLSI
Design presents state-of-the-art papers in VLSI design, computer-aided design, design analysis, design implementation, simulation and testing. Its scope also includes papers that address technical trends, pressing issues, and educational aspects in VLSI Design. The Journal provides a dynamic high-quality international forum for original papers and tutorials by academic, industrial, and other scholarly contributors in VLSI Design.
The development of microelectronics spans time which is even lesser than the average life expectancy of a human, and yet it has seen as many as four generations. Early 60’s saw the low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration in the late 60’s when around 100 transistors could be placed on a single chip.
It was the time when the cost of research began to decline and private firms started

entering the competition in contrast to the earlier years where the main burden was borne by the military. Transistor-Transistor logic (TTL) offering higher integration densities outlasted other IC families like ECL and became the basis of the first integrated circuit revolution. It was the production of this family that gave impetus to semiconductor giants like Texas Instruments, Fairchild and National Semiconductors. Early seventies marked the growth of transistor count to about 1000 per chip called the Large Scale Integration.

By mid-eighties, the transistor count on a single chip had already exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI. Though many improvements have been made and the transistor count is still rising, further names of generations like ULSI are generally avoided. It was during this time when TTL lost the battle to MOS family owing to the same problems that had pushed vacuum tubes into negligence, power dissipation and the limit it imposed on the number of gates that could be placed on a single die The second age of Integrated Circuits revolution started with the introduction of the first microprocessor, the 4004 by Intel in 1972 and the 8080 in 1974. Today many companies like Texas Instruments, Infineon, Alliance Semiconductors, Cadence, Synopsys, Celox Networks, Cisco, Micron Tech, National Semiconductors, ST Microelectronics, Qualcomm, Lucent, Mentor Graphics, Analog Devices, Intel, Philips, Motorola and many other firms have been established and are dedicated to the various fields in "VLSI" like Programmable Logic Devices, Hardware Descriptive Languages, Design tools, Embedded Systems etc.

In 1980s, hold-over from outdated taxonomy for integration levels. Obviously, influenced from frequency bands, i.e., HF, VHF, and UHF. Sources disagree on what is measured (gates or transistors)

SSI – Small-Scale Integration (0-102)

MSI – Medium-Scale Integration (102 -103)

LSI – Large-Scale Integration (103 -105)

VLSI – Very Large-Scale Integration (105 - 107)

ULSI – Ultra Large-Scale Integration (>= 107)

VLSI Technology, Inc. was a company which designed and manufactured custom and semi-custom ICs. The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose, California. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products. The company was founded in 1979 by a trio from Fairchild Semiconductor by way of Synertek - Jack Balletto, Dan Floyd, and Gunnar Wetlesen - and by Doug Fairbairn of Xerox PARC and Lambda (later VLSI Design) magazine.

II. LITERATURE SURVEY

"Low-power 19- transistor true single-phase clocking flip flop design based on logic structure reduction schemes"

In this paper, an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master-slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual VDD design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the powerdelay product (PDP). A TSMC 90-nm CMOS process was selected as the implementation

technology. In this paper, the performance levels of seven FF designs were compared. The timing parameters of each FF were first characterized. Post-layout simulation results indicated that the proposed design excelled in various performance indices such as PDP, clock-to-Q delay, average power consumption, and leakage power consumption. Moreover, the design was determined to have the smallest layout area. Compared with the conventional transmission-gate-based FF design, the PDP improvement in the proposed design was up to 63.5% (at 12.5% switching activity) and the area saving was approximately 10%. Further simulations on process corners, supply voltage settings, and working frequencies were conducted to study the design reliability.

" A power-efficient mixed-signal smart ADC design with adaptive resolution and variable sampling rate for low-power applications"

With the rapid development of portable electronics, wearable devices have become widely used to monitor body signals for long-term health care and home care applications. They detect vital signals through physiological sensors and then transmit them to a cloud database for evaluation and monitoring purposes through wireless communication systems. In this paper, a smart analog-to-digital converter (ADC) was realized by a mixed-signal application-specific integrated circuit (ASIC) based on adaptive resolution and lossless compression techniques for electrocardiogram (ECG) signal monitoring. The sampling clock for the ADC can be adaptively selected according to the characteristic of the signals. The lossless encoder consists of trend forecasting and entropy coding modules. The transmission data rate was decreased efficiently by adaptive resolution and lossless compression techniques. The chip aims to meet the low power consumption for the design, because it reduced the signal transmission rate and maintained high-quality ECG signal detection. The proposed mixed-signal ASIC design was realized using a 0.18-μm CMOS process with a total power consumption of 78.8 μW when operating at 1 kHz and a total chip area of 850×850 μm 2 .

"Fully functional operation of low-power 64-kb Josephson-CMOS hybrid memories"

We have been developing a Josephson-CMOS hybrid memory with subnanosecond access time in order to overcome the memory bottleneck in single-flux-quantum digital systems. In this study, we aimed for reducing the power consumption of the 64-kb CMOS static RAM. We took three approaches, miniaturization of memory cells, improvement of data drivers, and employment of a binary-tree decoder. By using these techniques, we decreased the power consumption of 64-kb CMOS static RAMs by 54% in the write operation and by 8% in the read operation. Moreover, we aimed for demonstrating the fully functional operation of the 64-kb Josephson-CMOS hybrid memory composed of the low-power CMOS static RAM, Josephson interface circuits, and Josephson current sensors by using the Rohm 0.18 μm process and the AIST standard process 2. We confirmed the correct memory operation for arbitrary address accesses at low speed. The total access time was evaluated to be 1718 ps and the power consumption was estimated to be 27.62 mW in the write operation and 21.25 mW in the read operation in circuit simulations. Based on these estimations, we discuss the access time and the power consumption of hybrid memories using future CMOS processes.

III.EXISTING ARCHITECTURE:

DESIGN OF CMOS PHASE DETECTOR CIRCUIT AND PHASE-FREQUENCY DETECTOR CIRCUIT In this section the circuit of phase detection and phase frequency detection has been designed using

CMOS technology. A .Phase Detector shows the CMOS based phase detection circuit. In this circuit two input XOR gate has been constructed following CMOS technology. T-SPICE tools is used to simulate the circuit . Input waveforms and output waveforms are presented in Fig. 2. The waveforms at output side represent the duration of phase between the two input waveforms. This means whenever two input wave forms (A and B) are out of phase the output is at logic high. In this example the phase difference between input waveforms are measured as 10 ns , from the output wave form

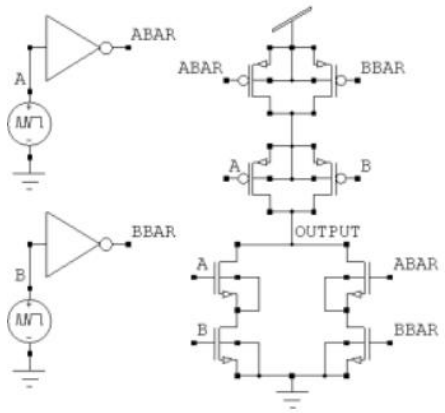


Fig.1. CMOS Phase Detector Circuit

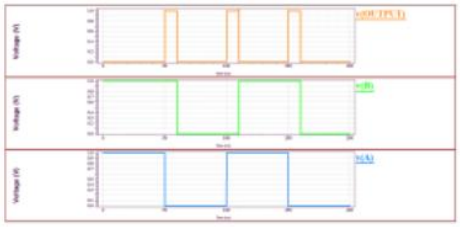
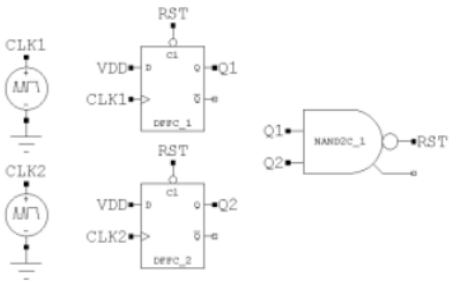


Fig.2. Input and output waveform from phase detector circuit

B. Phase-Frequency Detector The diagram of one conventional phase-frequency detector [10] using two D flip-flop and one NAND gate is presented in Fig.3. D input of both the flip-flop are connected to supply voltage VDD. Based on the clock input, output of the flip-flop has been generated. The input and output signal are shown in Fig. 4. According to this design, CLK1 is in leading phase than CLK2 signal. Q1 output indicates the phase detection between two Signal CLK1 and CLK2. In this example the phase difference between two clock signal has been measured as 10 ns .



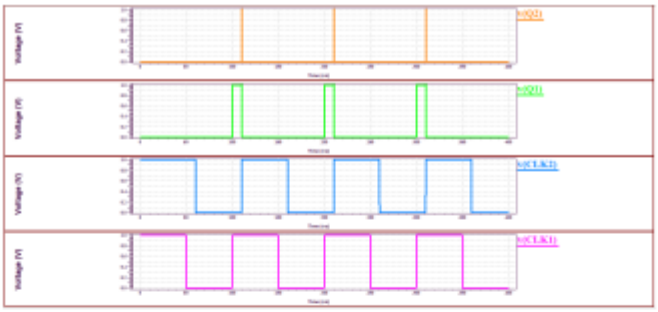


Fig.4. Phase detection by the circuit diagram of Fig.3

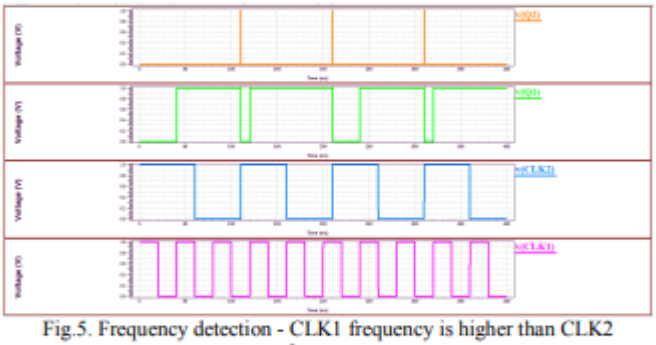
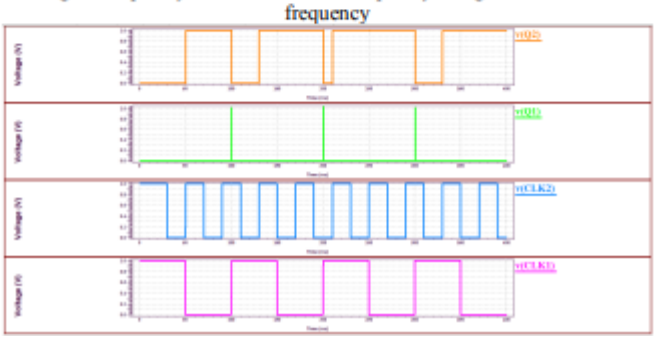


Fig.5. Frequency detection - CLK1 frequency is higher than CLK2 frequency



The circuit of Fig.3 is also useful to detect frequency. Whenever CLK1 frequency is higher than CLK2 then many pulses are produced at Q1 node as shown in Fig.5. On the other hand whenever CLK2 frequency is higher than CLK1, then many pulses are generated at Q2 node as shown in Fig. 6 .

IV.PROPOSED ARCHITECTURE:

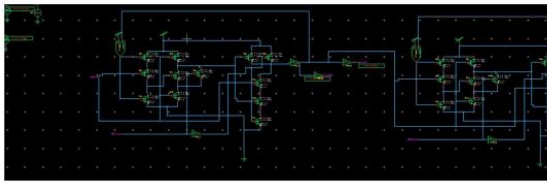
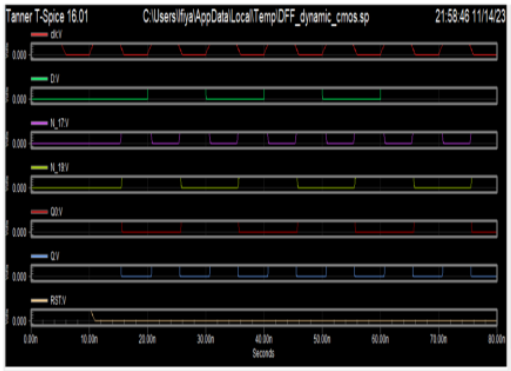
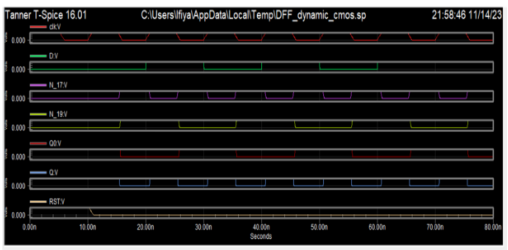


Fig.4.1 phase frequency detector



This architecture is more complex than the basic "Bang-Bang" PFD and is often used in more sophisticated PLL designs. It provides higher precision and accuracy in phase and frequency detection, allowing for better control of the VCO and consequently tighter frequency synchronization between signals. The design and implementation of PFDs can vary significantly based on specific requirements such as frequency range, phase accuracy, power consumption, and integration with other components within the system. Advanced PFD designs might include digital signal processing elements for improved performance in various applications.

V.RESULT:



VI.CONCLUSION

In this work the phase detector circuit has been designed using MOS transistor with length of 22 nm and 16 nm. The power dissipation, gate delay and PDP of phase-frequency detector circuit is measured at channel length of 150nm. In case of phase detector, design using 22 nm channel length is preferred over 16 nm design context to average power consumption and PDP. However for high speed design 16 nm technology is better than 22 nm technology. On the other side for low power design of phase-frequency detector, small value of VDD is preferred however higher value of VDD provides better speed performance . The reported value of results in this paper context to power dissipation, speed and PDP, reference to recent work are agreeable for the design of VLSI circuits with low power dissipation and fastest speed.

Existing Architecture	Proposed Architecture
Power: $VV_1 = 1.8 \times 10^{-6}$ $VV_2 = 1.5 \times 10^{-6}$ Avg $= \frac{3.3}{2}$ $= 1.65 \times 10^{-6}$ watts ➢ **Delay = 406.018 ps** ➢ High Delay ➢ Low speed	**Power:** $VV_1 = 1.8 \times 10^{-6}$ $VV_2 = 2.2 \times 10^{-6}$ Avg $\frac{vv1+vv2}{2} = \frac{(1.8+2.2)}{2} 10^{-6}$ $= 2.0 \times 10^{-6}$ watts ➢ **Delay – 3.20ns** ➢ Low Delay ➢ High speed

VII.FUTURE SCOPE:

The future scope of CMOS phase detectors is promising, with many researchers working on improving their design and performance. One of the recent developments in the design techniques of CMOS phase detectors is the use of both linear and nonlinear phase detectors. These techniques have been shown to have been shown to have advantages such as improved sensitivity to input data pattern and reliability

REFERENCES

[1] J-F Lin , M-H Sheu , Y-T Hwang , Chen-Syuan C-S Wong ,M-Y Tsai Y, “Low-power 19- transistor true single-phase clocking flip flop design based on logic structure reduction schemes” , Trans. on Very Large Scale Integration (VLSI) System , IEEE ,Vol. 25 , No. 11 ,pp. 3033–3044 ,2017.

[2] S-L Chen , JF Villaverde , H-Y Lee , DW-Y Chung, T-L Lin ,C-H T seng , K-A Lo, “ A power-efficient mixed-signal smart

ADC design with adaptive resolution and variable sampling rate for low-power applications" , IEEE Sensor Journal , Vol. 17, No. 11,pp.3461–3469 ,2017.

[3] G Konno , Y Yamanashi , N Yoshikawa , "Fully functional operation of low-power 64-kb Josephson-CMOS hybrid memories" , IEEE Trans Appl. Supercond. , Vol. 27 , No.4 , 1300607 ,2017.

[4] R Rajaei , SB Mamaghani , "Ultra-low power, highly reliable, and nonvolatile hybrid MTJ/CMOS based full-adder for future VLSI design" ,EEE Trans Device and Material Reliability , Vol. 17 , No. 1 , pp.213–220 , 2017.

[5] Z Zhang , J Yang , L Liu , P Feng P, J Liu ,N Wu "A 0.9–2.25-GHz Sub-0.2-mW/GHz compact low-voltage low-power hybrid digital PLL with loop bandwidth-tracking technique", IEEE Trans Very Large Scale Integr (VLSI) Syst , Vol.26 , No.5 , pp. 933–944, 2018

[6] D. Das , VLSI Design , Oxford University Press, New Delhi , India , 2010,pp. 163-199.

[7] A.Sarkar, S.De ,C.K. Sarkar , VLSI Design and EDA Tools , SCITECH Publications (India) PVT. LTD. , India , 2011,pp. 6.1-6.10.

[8] S-M Kang ,Y Leblebici ,CMOS Digital integrated circuits analysis and design ,TMH, New Delhi ,India , 2003 ,pp.287-294.